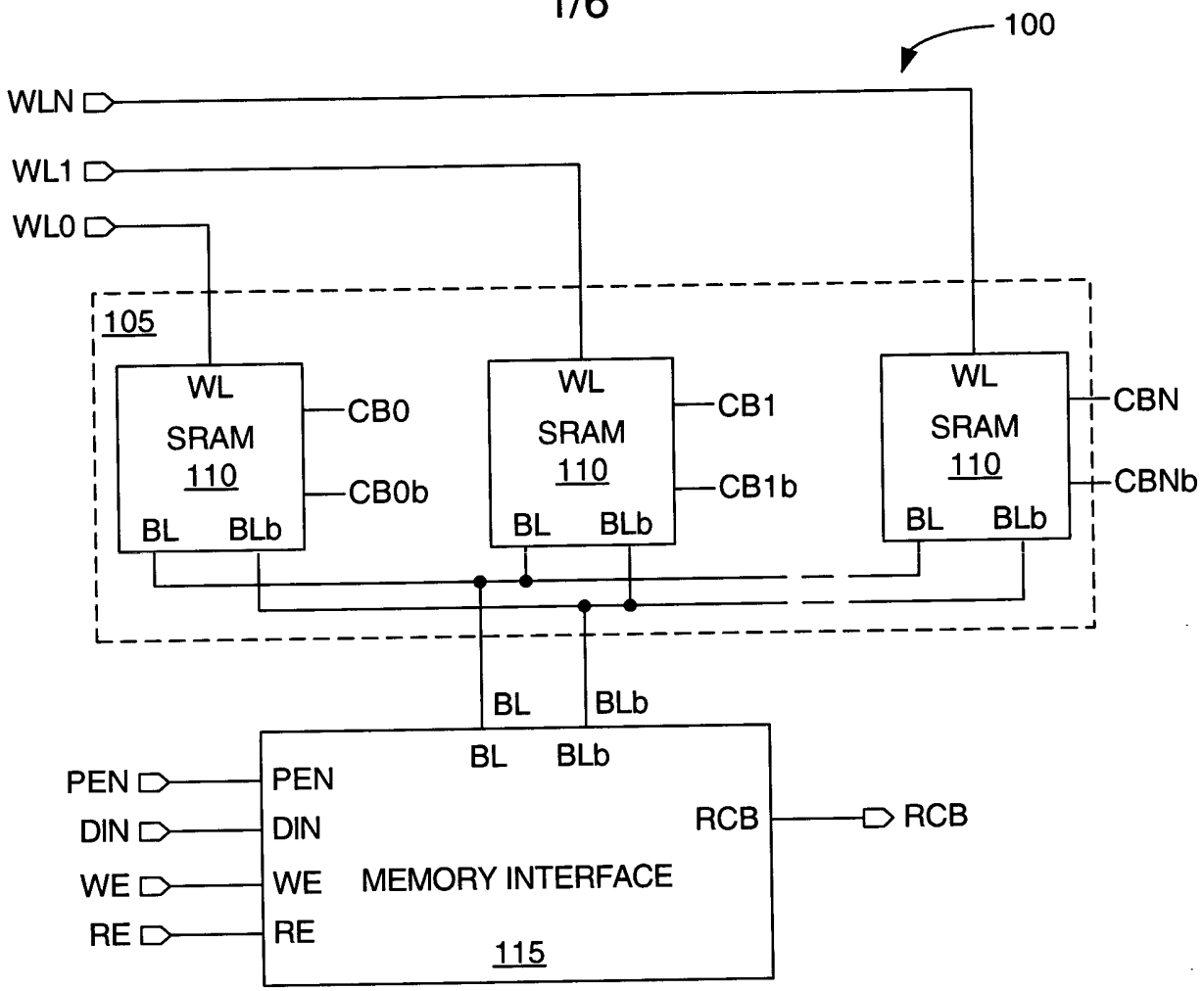

FIG. 1 (PRIOR ART)

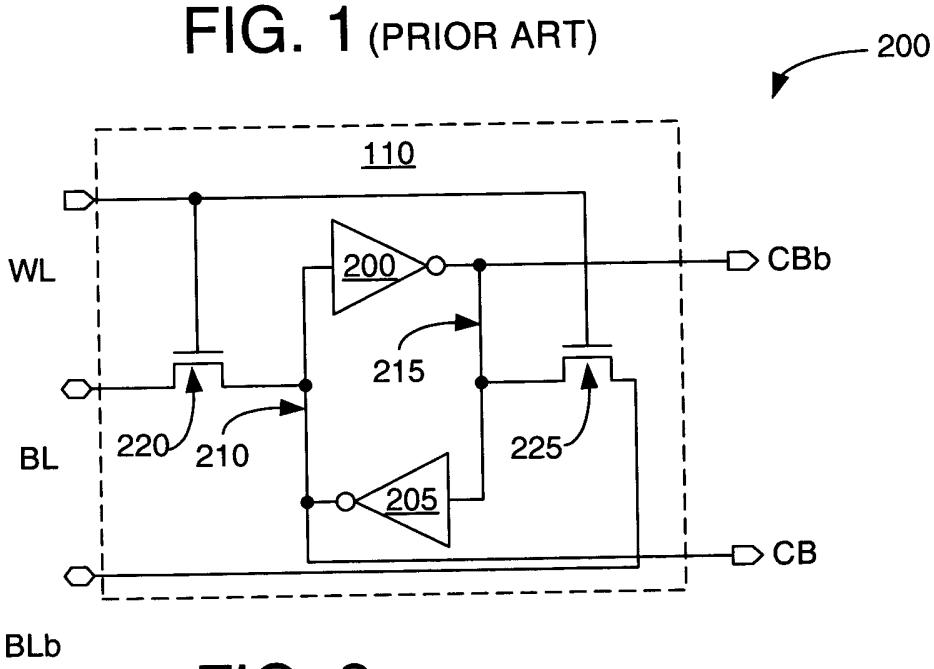

FIG. 2 (PRIOR ART)

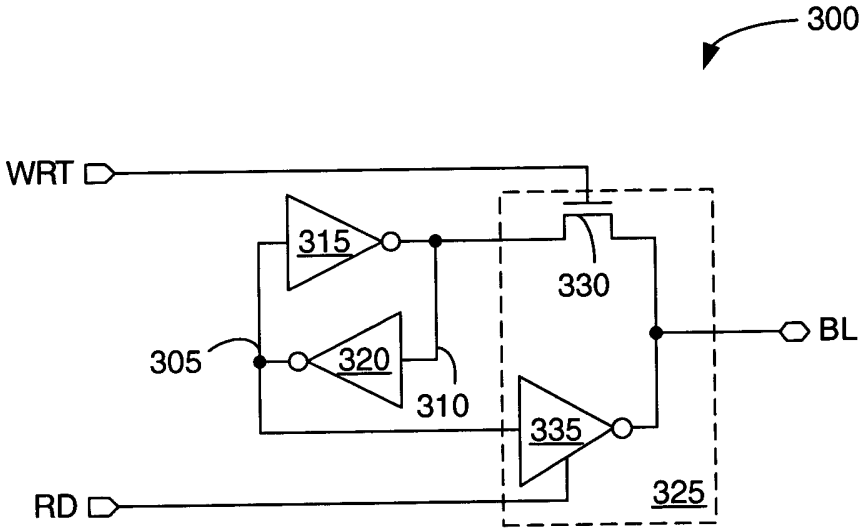
300
WRT
315
330
BL
305
320
310
335
RD
325

FIG. 3

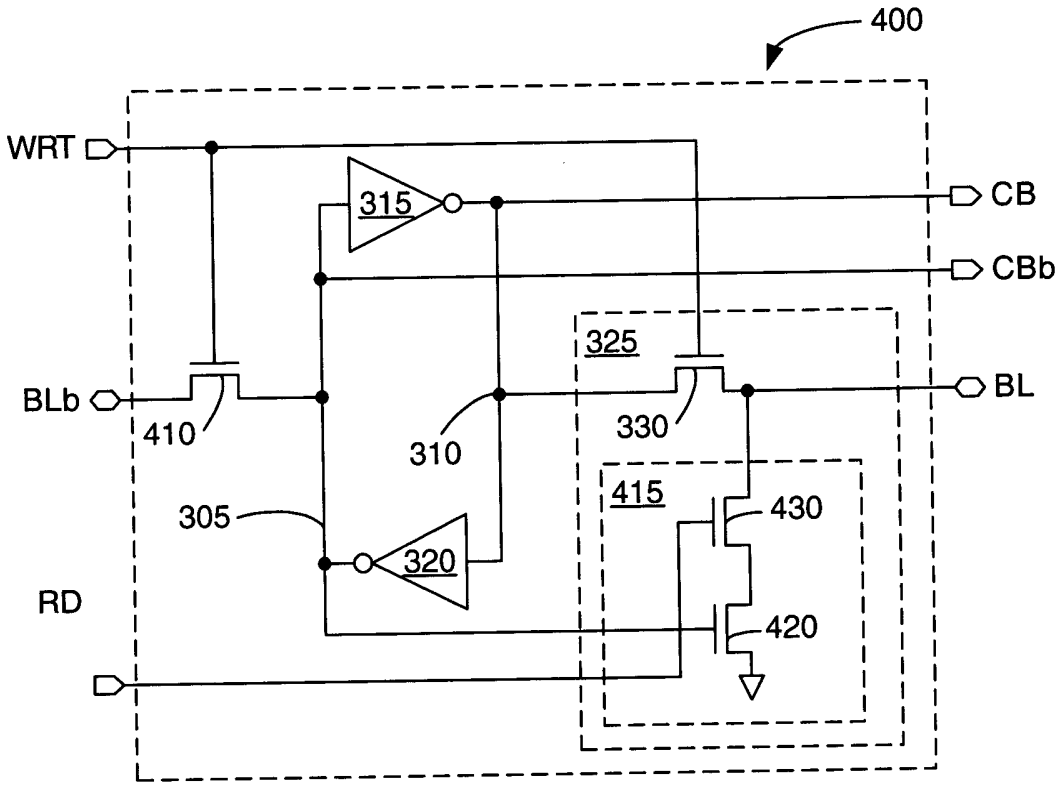
400
WRT
315
CB
CBb
325
BLb
410
310
330
BL
415
305
430
320
RD
420

FIG. 4

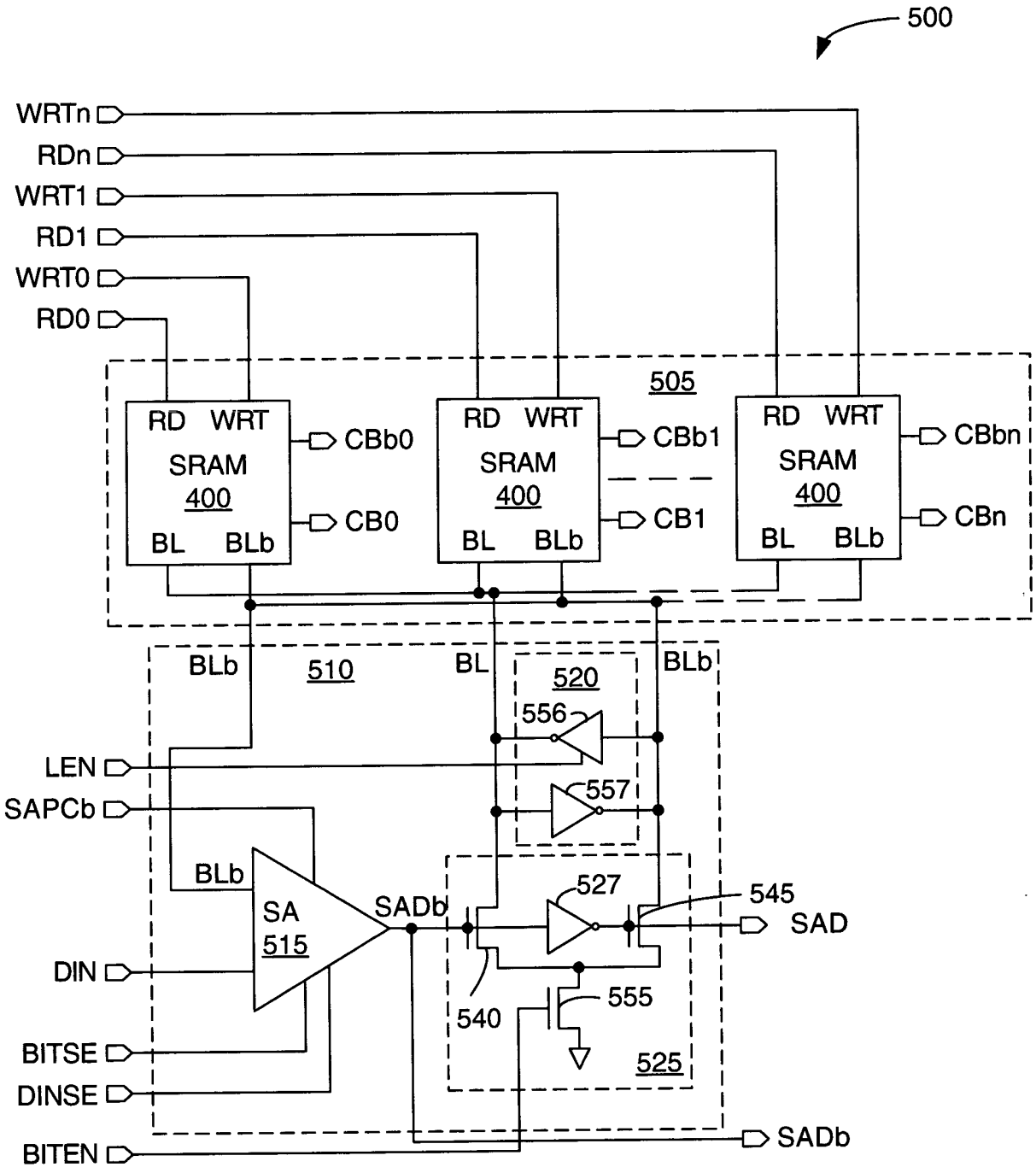
500
WRTn
RDn
WRT1
RD1
WRT0
RD0
505
RD WRT
SRAM
400
BL BLb
CBb0
CB0
CBb1
CB1
CBbn
CBn
BLb
510
BL
520
556
557
LEN
SAPCb
BLb
SA
515
SADb
527
545
SAD
DIN
540
555
525
BITSE
DINSE
BITEN
SADb

FIG. 5

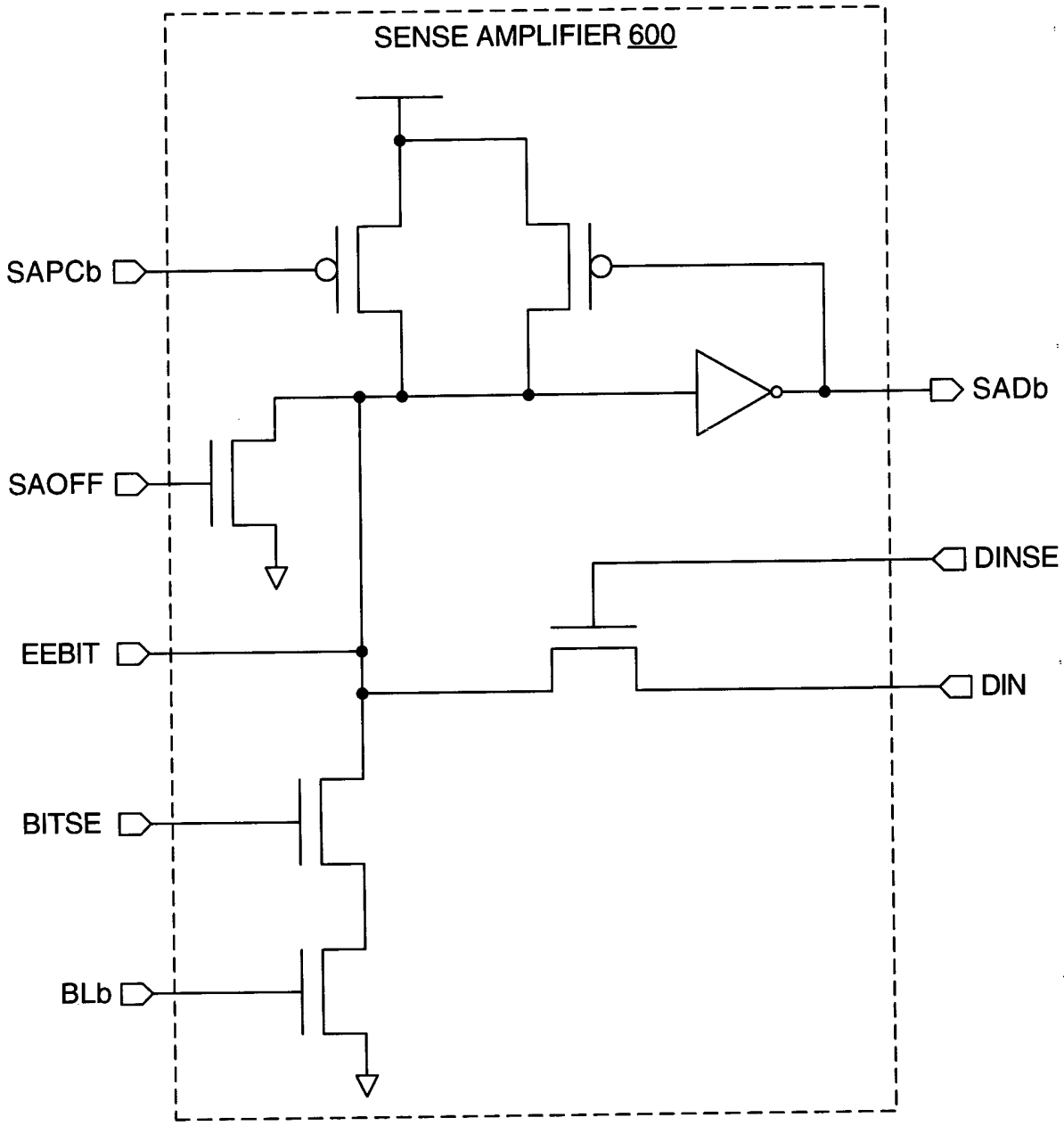
SENSE AMPLIFIER 600
SAPCb
SADb
SAOFF
DINSE
EEBIT
DIN
BITSE
BLb

FIG. 6

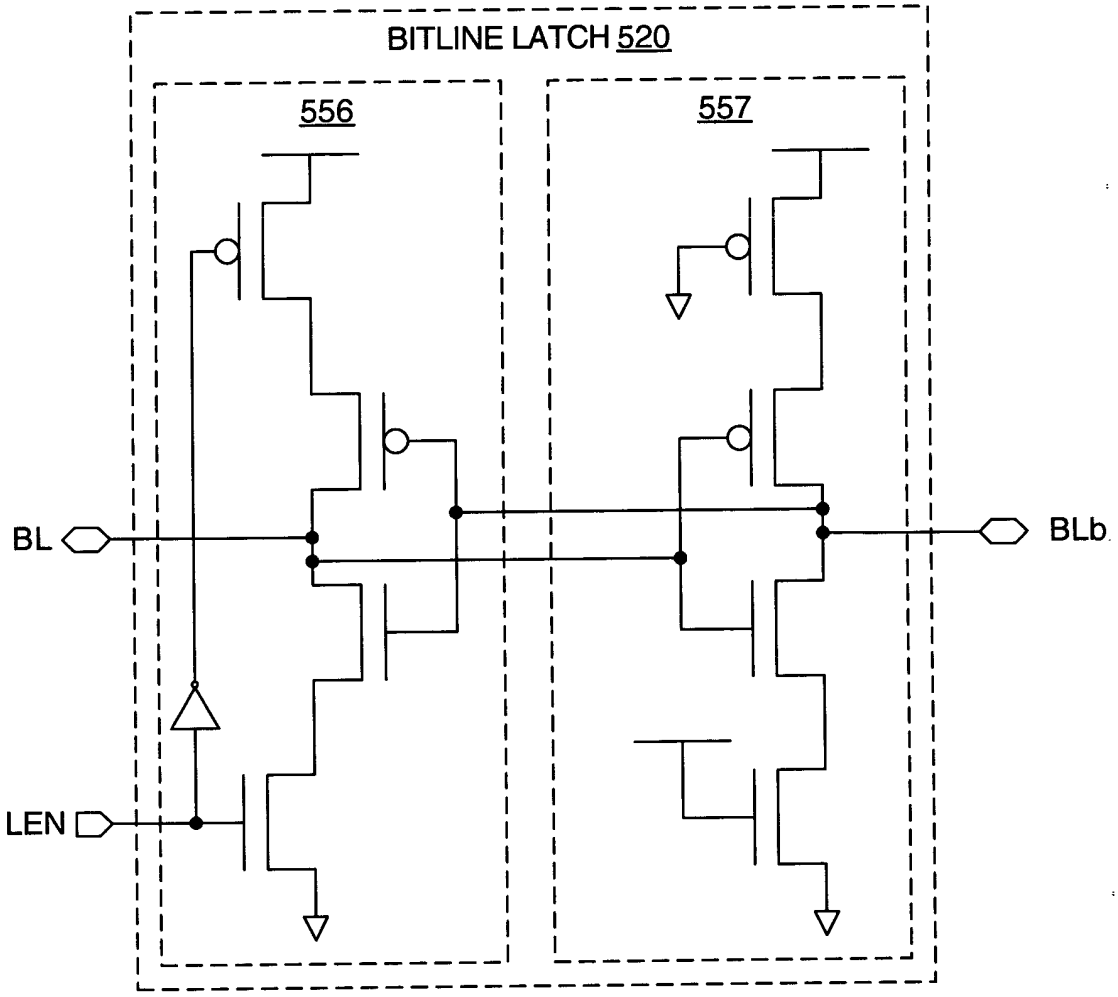

FIG. 7

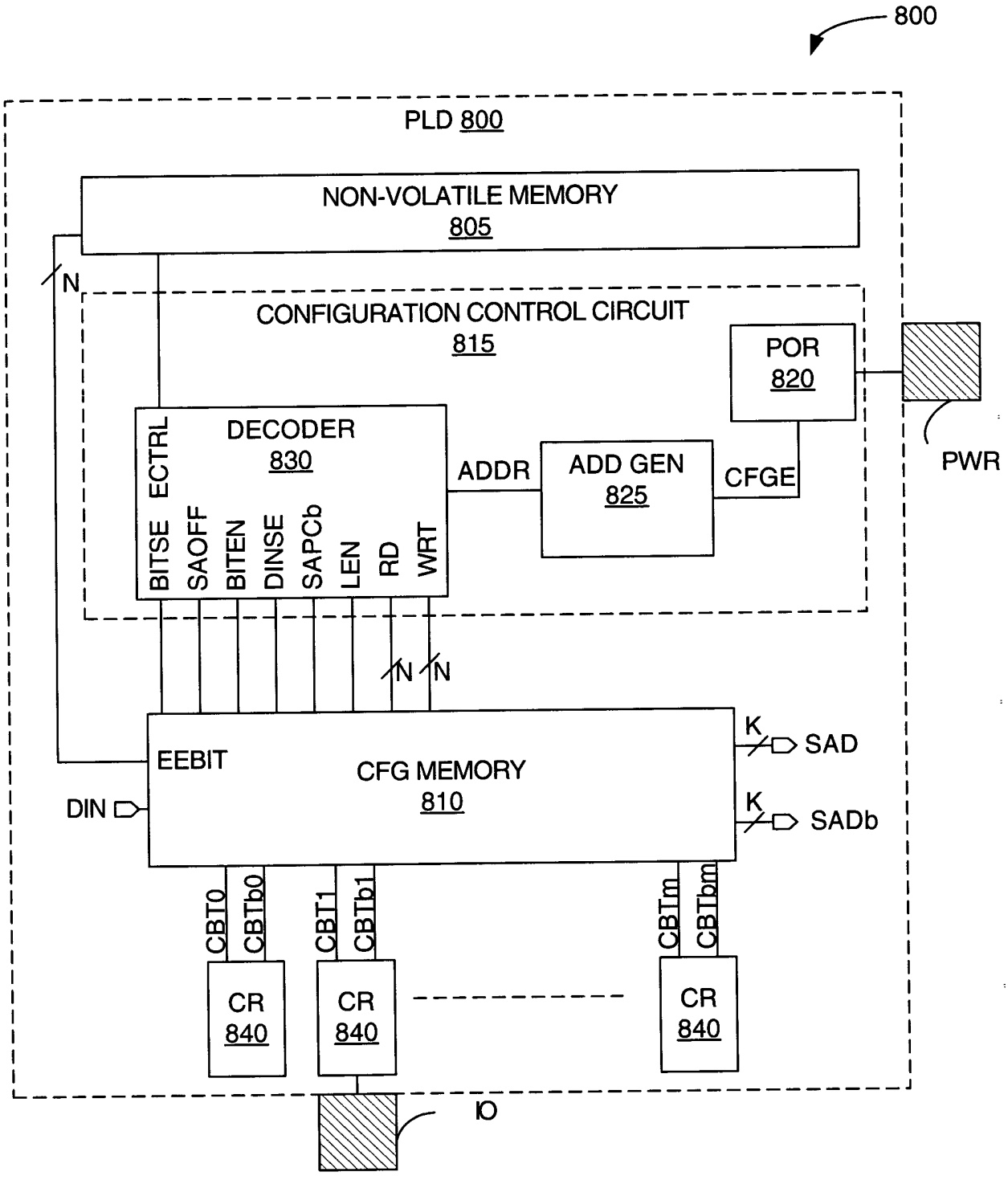
800
PLD 800
NON-VOLATILE MEMORY
805
N
CONFIGURATION CONTROL CIRCUIT
815
POR
820
PWR
DECODER
830
ECTRL
BITSE
SAOFF
BITEN
DINSE
SAPCb
LEN
RD
WRT
ADDR
ADD GEN
825
CFGE
N
N
K
SAD
EEBIT
CFG MEMORY
810
DIN
K
SADb
CBT0
CBTb0
CBT1
CBTb1
CBTm
CBTbm
CR
840
CR
840
CR
840
IO

FIG. 8